

Z-100 LifeLine

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Z-204 Multiport Input/Output Card Manual

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Z-204 Multiport I/O Board

The Heath/Zenith Z-204 Multiport Input/Output Card for the Z-100

Source: The following information was taken from the Zenith Data Systems' "Z-204-RD Multiport Input/Output Card" Manual and its Service Manual.

The Multiport Input/Output (I/O) Card with Ring Detect expands the capability of the Z-100 series computer by providing three additional serial I/O ports and one limited handshaking asynchronous output port. It is completely configurable by a set of numerous jumpers to several RS-232 or S-100 bus configurations and may be installed in any vacant S-100 bus card slot.

Three cables were provided with the board for connecting the card to the backplate. Two cables were used for synchronous/asynchronous DTE communication, and the third cable was for DCE communication. Additional cables for DCE, DTE, and parallel were available, if needed.

All the information needed to use this I/O card is contained in this manual. Please read it carefully before you attempt to install or use your multiport I/O card.

Specifications:

- 4 Serial I/O Ports
 - * Port 1: RS-232 Asynchronous, DTE or DCE.
 - * Port 2: RS-232 Asynchronous, DCE
 - * Port 3: RS-232 Asynchronous, synchronous (SDLC, BDLC, BISYNC, CCITT X.25); DTE or DCE
 - * Port 4: Limited, asynchronous, DCE
- 2 Parallel Ports
 - 1 Buffered TTL Parallel Input Port, Used for sensing ring detect on RS-232 ports

 - * 1 Buffered TTL Centronics-compatible parallel output port.

Addressing

* Jumper-selectable 8-bit or 16-bit addressing on 32-byte boundaries

Serial I/O Device Type * 2 Signetics 2661-2 EPCI's; 1 Intel 8274 (or NEC7201) MPSC

Parallel I/O Device Type * 1 Intel 8255A PPI

Vector Controller Chip * 1 Intel 8259A PIC

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Access Time
    * 250ns maximum
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Wait States

* 0, 1, or 2; jumper-selectable

Interrupt Operation * Jumper-selectable; VIO* through VI7*

Bus Interface * S-100, IEEE Standard 696

Power Requirements * 8-11 volts DC at 1.0A maximum * + 16 volts at 275ma * - 16 volts at 125ma

Hardware Requirements:

Host Computer Requirements

The Multiport Input/Output Card can be used with any host computer that meets IEEE #696 (S-100 Bus) interface requirements.

H/Z-100 Computer Requirements

You can install the Input/Output Card in any open slot in the card cage of your H/Z-100 Computer.

The Input/Output Card is compatible with other Zenith Data Systems' interface cards designed for your computer. You do not need to make any changes to your CPU board to accommodate it. Just follow the installation instructions given in this manual.

Configuration:

The following instructions are divided into two sections. Use the "Typical Configuration" section to set up the jumpers and switches as they were when they left the factory. If your needs are different from those met by this configuration, use the information provided in the "Detailed Configuration Data" section.

Typical Configuration

The following instructions will configure your Input/Output Card for operation at address 060h, with no wait states inserted by the card. (The Heath/Zenith H/Z-100 computer automatically inserts a wait state whenever it executes an input or output instruction.)

Note: In wired products, the factory presets this card to a configuration in which the serial I/O channels function as follows:

* Channel 1	- Asynchronous
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- * Channel 2 Asynchronous
- * Channel 3 Asynchronous or synchronous
- * Channel 4 Limited asynchronous

If a card has been configured to some other specifications, you can return it to the original factory specifications by using the following procedure.

Refer to Pictorial 1 for the following steps.

[] Position card as shown, with edge connector P101 toward you.

Verify that jumpers are in the correct locations, as shown in Pictorial 1. Use this check list to be sure only these jumpers for this preset situation are installed.

 $[\]$ Place a jumper on the left & center pins of J102 to provide 8-bit addressing.

[] Place a jumper on J101A to select VIO* interrupt operation.

 $[\]$ Place a jumper on the bottom & center pins of J109 to ground DCD on U117.

[] Place a jumper on the bottom and center pins of J110 to ground CTS on U117.

 $\left[\right]$ Place a jumper on J112 to connect TXD from U118 to U126.

 $\left[\right]$ Place a jumper on J113 to connect RXD from U127 to U118.

[] Place jumpers on the bottom and center pins of J114 and J115 to connect the Carrier Detect and Clear to Send pins of Channel B on U118 to ground.

[] Place jumpers on J127 and J128 to connect the Transmit and Receive Clock lines for Channel A on U118 to the outputs of baud rate generator U119.

[] Place jumpers on J125 and J126 to provide Transmit and Receive Clocks on P104.

[] Place jumpers on J129 and J130 to connect the Transmit and Receive Clock lines for Channel B on U118 to the outputs of baud rate generator U120.

[] Place a jumper on J111 to connect the interrupt line from the interrupt controller to the LED driver for D102. This LED indicates the status of the interrupt line.

[] Place a jumper on J104. This provides a Strobe Signal required to operate U135 in mode 1. Use pins 1 and 2 to select Internal Strobe (from pin 6 of U135) or pins 2 and 3 to select External Strobe (from pin 10 of P107).

[] On DIP switch SW102, set switches 2 and 3 in the OFF position. Set switches 1 and 4 in the ON position. This sets the card to operate at address 060h.

 $[\]$ Set all other switches on SW102 and SW101 to the OFF position.

Detailed Configuration

Use the following information to configure the Multiport Input/Output Card for use with non-Heath/Zenith S-100 bus microcomputers, and for customized applications to $\rm H/Z-100$ computers.

Jumper Location:	Jumper ON or OFF:	Functional Result:
J102	ON left & ctr pins ON ctr & right pins	<pre>16-bit addressing selected. 8-bit addressing selected.</pre>
J103	Jumper OFF ON left & ctr pins ON ctr & right pins	Zero wait state selected. One wait state selected. Two wait states selected.



OPTION #1

For asynchronous operation of Channel 1 (U116), leave jumpers OFF J105, J131, J134, J132, and J106.

OPTION #2

Channel 1 (U116) can not be used synchronously.

OPTION #3

For asynchronous operation of Channel 2 (U117), use the following jumper configuration, as required, to interface with serial printers using different "Printer Ready" handshaking:

Jumper Location:	Jumper ON or OFF:	Functional Result:
J135	Jumper ON or OFF	ON selects RTS signal from DTE OFF if there is no external handshake.
J136	Jumper OFF	
J133	ON ctr & right pins ON left & ctr pins	Selects non-inverted RTS. Selects inverted RTS.
J109	ON ctr & lower pins ON ctr & upper pins	DCD grounded. DCD connected to RTS.
J110	ON ctr & lower pins ON ctr & upper pins	CTS grounded. CTS connected to RTS

OPTION #4

Jumper J107 is configured for Interrupt Operation of U116, and Jumper J108 is configured for interrupt Operation of U117:

Jumper Location:	Jumper ON or OFF:	Functional Result:
J107	Jumper ON	Interrupts on TXRDY or TXEMPTY.
	Jumper OFF	Interrupts on TXRDY.
J108	Jumper ON	Interrupts on TXRDY or TXEMPTY.
	Jumper OFF	Interrupts on TXRDY.

OPTION #5

For asynchronous operation of Channel 3 (U118), use the following configuration:

Jumper Location:	Jumper ON or OFF:	Functional Result:
J112	Jumper ON	Connects TXD to RS-232 driver.
J113	Jumper ON	Connects RXD to RS-232 receiver.
J127	Jumper ON	Selects TXCA from U119.
J128	Jumper ON	Selects RXCA from U119.
J117	Jumper OFF	Disconnects external Transmit Clock.
J118	Jumper OFF	Disconnects external Receive Clock.

J125	Jumper ON or OFF	If ON, provides Transmit Clock on P104, pin 4.
J126	Jumper ON or OFF	If ON, provides Receive Clock on P104, pin 2.

OPTION #6

For synchronous operation of Channel 3 (U118), use the following configuration:

Jumper Location:	Jumper ON or OFF:	Functional Result:
J112	Jumper ON	Connects TXD to RS-232 driver.
J113	Jumper ON	Connects RXD to RS-232 receiver.
J127	Jumper OFF	Disconnects TXCA from U119.
J128	Jumper OFF	Disconnects RXCA from U119.
J117	Jumper ON	Connects external Transmit Clock.
J118	Jumper ON	Connects external Receive Clock.
J125	Jumper OFF	Disconnects Transmit Clock from P104, pin 4.
J126	Jumper OFF	Disconnects Receive Clock from P104, pin 2.

OPTION #7

In the Interrupt-driven Mode, one and only one of jumpers J101A through J101H can be used. If the card is prewired at the factory, it is configured with a jumper on J101A. Interrupt line selection is as follows:

Jumper Location:	Jumper ON or OFF:	Functional Result:
J101A	Jumper ON	Selects S-100 bus Interrupt Line VIO*.
J101B	Jumper ON	Selects line VI1*.
J101C	Jumper ON	Selects line VI2*.
J101D	Jumper ON	Selects line VI3*.
J101E	Jumper ON	Selects line VI4*.
J101F	Jumper ON	Selects line VI5*.
J101G	Jumper ON	Selects line VI6*.
J101H	Jumper ON	Selects line VI7*.

OPTION #8

If you desire, you can set up a monitor of the Interrupt Line by placing a jumper on J111. This connects the Interrupt Line to D102. As shown on the schematic, the right-hand pin of J111 is connected to the LED driver for D102, which permits use of an external probe (not supplied) in conjunction with D102 for trouble shooting purposes.

Table 1. (Address Switch Settings)

<u>Swi</u>	tch #		<u>Swit</u>	ch Po	sitio	ns				
SW1(Addi	01 r Bit		1 A15	2 A14	3 A13	4 A12	5 A11	6 A10	7 A9	8 A8
SW1(02		A7	A6	A5	A4				
Exa To fol	mple set i lows	of S up ar :	Switc n add	ch Se lress	tting of (g :)660h	, set	: swi	.tch	es as
	SI	v101								
	1	2	3	4	5	6	7	8		
	ON	ON	ON	ON	ON			ON		
						OFF	OFF			
	A15	A14	A13	A12	A11	A10	Α9	A8		

AID	AI4	ALS	AIZ	AII	AIU	4
SI	W102					
1	2	3	4			
ON			ON			
	OFF	OFF				
Α7	A6	A5	A4			

Installation

WARNING: When the line cord is connected to an AC outlet, hazardous voltages can be present inside your computer. ALWAYS turn OFF the computer and disconnect the line cord before opening the computer.



[] Refer to Pictorial 2 and remove the top cover from your H/Z-100 computer. Unlatch the cover, as shown, pull the metal side slides all the way back and then push cover forward and lift off the base. Set the cover aside.

[] Unlatch and remove all cables in the card cage to provide ample work space while inserting your Multiport I/O Card.

Refer to Pictorial 3a through 3c for the following steps.



[] Refer to Detail 3b, mount the D-connector of DCE cable (134-1393) at location J12 on the rear panel of your computer, using two 4-40 spacers, two #4 lock washers and two 4-40 nuts.

[] Route the free end of the cable over the Z-100 card cage and plug it into the second of the four 15-pin right-angle connectors on the top of the card. Use the connector that corresponds to the serial port you plan to use.

[] Using a procedure similar to the one just described, install the two DTE cables for synchronous/asynchronous communication from J13 to the first 15-pin connector and J11 to the third one.

 $[\]$ If you desire to install a Parallel Port cable, refer to Pictorials 3a and 3c.



[] With Z-204-RD card installation completed, reinstall any cables you removed earlier to provide workspace.

[] With all cables installed, reinstall the top cover on your $\rm H/Z{-}100$ computer.



Refer to Pictorial 4, the Z-204 Block Diagram, as you read this description.

The Multiport Input/Output Card is divided into the following six sections:

- 1. The Data Bus Buffers
- 2. System Decode Control
- 3. Four (4) Serial I/O Channels
- 4. Parallel I/O Channels, (one of each)
- 5. Interrupt Control
- 6. Wait State Generator

Data Bus Buffers - Buffer the DOO - DO7 and the DIO - DI7 lines on the S-100 bus. When enabled, the buffers provide a data path between the S-100 bus and the internal data bus on the card.

System Decode Control - Contains the logic required to perform address decoding, to generate control signals (needed for the various onboard peripheral chips), and to enable the data bus buffers.

Serial I/O Channels - The Z-204 Card contains four Serial I/O Channels. These channels can be configured in the following manner.

Note: Table 2 provides a tabulation of the features for each channel.

Channel 1 can be configured as a DCE or DTE port. It can be used in asynchronous mode only and it can be interrupt driven or polled.

Channel 2 is configured as a DCE channel. It can be used in the asynchronous mode only. The channel is jumper-configurable to accommodate the variations in "Printer Ready" handshake signals from different manufacturers. It can be interrupt-driven or polled.

Channel 3 can be configured as a DTE or DCE channel. It can be used in asynchronous or synchronous modes and it can be interrupt-driven or polled.

Channel 4 provides a limited DCE channel, asynchronous only since it receives the internal ring-detect circuitry.

1	Cable	≥ 2	
Serial	I/0	Channel	Configurations

<u>Configurations</u>	<u>Serial I/O Channels</u>					
DCE Channel	1 Yes	2 Yes	3 Yes	4 Yes		
DTE Channel	Yes	No	Yes	No		
Asynchronous	Yes	Yes	Yes	Yes		
Synchronous	No	No	Yes	Yes		
Interrupt- Driven or Polled	Yes	Yes	Yes	Yes		

Parallel Input and Output Channels - This section of the card contains one parallel input port and one parallel output port. Both ports are buffered.

The parallel input port is used for sensing ring detect on the RS-232 ports; one bit is used for DSR and three bits are used for ring detect. The other four bits are available for parallel input.

The parallel (8-bit) output port provides latching and handshaking functions and is capable of interrupt-driven operation with handshaking. It is also compatible with the Centronics interface.

Interrupt Control - The interrupt lines from the serial communication chips and parallel I/O are connected to the seven input lines of the Interrupt Controller. Level 7 (IR7) on the 8259 IC (U112) is disabled. The interrupt controller combines the internal card interrupts into one jumper-selectable S-100 bus interrupt. When an interrupt occurs, the interrupt controller supplies a vector, under software control, which can serve as a pointer for a multiport I/O handler routine.

Wait State Generator - The Z-204 card is jumperselectable to generate either zero, one, or two wait states.

System Decode and Control

U103 and U104 are address bus buffers which buffer the S-100 bus address lines. The outputs from the address bus buffers go to U105 and U106 which, as 8-bit comparators, compare the address output on the address bus with the address set on switches SW101 and SW102.

When the received address on the card matches the address set on the switches, a Board Select Signal (BDSEL) is generated. It is important to note that the card will respond only to input or output instructions. A Board Select Signal will be generated when the address in the second byte of the I/O instruction matches the address set on the card.

The card can be configured for either an 8-bit or 16-bit addressing mode with jumper J102.

When the jumper is placed on pins 1 and 2 (left & center) of jumper J102, pin 19 on U105 is connected to pin 1 of U106, selecting 16-bit addressing. When the jumper is placed on pins 2 and 3 (center and right) of J102, pin 1 on U106 is grounded. This condition selects the 8-bit addressing mode.

Address bits A0 through A4 are not used in the address comparison. These address bits are used as follows:

* A4 is used to select the upper or lower half of the one out-of-four decoder, U132.

 $\,$ A2 and A3 are used as the address inputs for the decoder U132.

 $\,$ \star A0 ad A1 are used to select the internal registers of the LSI chips used on the card.

Table 3 gives an example of how A0 and A1 are used to select the internal registers of the 2661 (U116 and U117) Enhanced Programmable Communications Interface (EPCI).

Table 3 EPCI (2661/U116, U117) Register Addressing

A1	AO	Register Selected
0	0	Data Register
0	1	Status Register
1	0	Mode Registers
1	1	Command Register

The card occupies a 32-byte address space. For this reason, whenever two or more cards are used in the same system, each card can be stacked 32 addresses apart. The card address must start at even boundaries; e.g., 00h, 20h, 40h, 60h, etc.

For a description of the function of each address within the 32-byte address space, refer to Table 4.

Table 4 Address Space Description

Base	Address	Desc	ription
+	00h	2661	Data Register for (U116)
+	01h	2661	Status Register (U116)
+	02h	2661	Mode Registers (U116)
+	03h	2661	Command Register (U116)
+	04h	2661	Data Register for (U117)
+	05h	2661	Status Register (U117)
+	06h	2661	Mode Registers (U117)
+	07h	2661	Command Register (U117)
+	08h	1943	Baud Rate Clock CH/A (U119)
+	0Ch	1943	Baud Rate Clock CH/B (U120)
+	10h	8259	INTA Port (U112)
+	14h	8259	ICW and OCW Select (U112)
+	15h	8259	ICW and OCW Select (U112)
+	18h	8255	Port A Select (U135)
+	19h	8255	Port B Select (U135)
+	1Ah	8255	Port C Select (U135)
+	1Bh	8255	Control Port (U135)
+ + +	1Ch 1Dh 1Eh 1Fh	8274 8274 8274 8274	Channel A Data Port (U118) Channel B Data Port (U118) Channel A Command Port (U118) Channel B Command Port (U118)

Note: U107 buffers the control signals from the S-100 bus.

When the card is selected and an input or output instruction is executed, pin 8 of U109 (BIOSEL) goes high. If both address line A4 and U109 pin 8 are high, the upper half of the decoder U132 is selected.

The upper half of decoder U132 selects chips that work with timing based on an Intel type bus, as shown in Pictorial 5. In this case, note that the CS pulse is active before the RD or WR pulse.



The lower half of the decoder selects the EPCI's and the baud rate generators. The timing for these chips is based on a Motorola type bus, as shown in Pictorial 6. In this case, note that the R/W (RD/WR) line is active before the CS pulse. (Note: Pen in lines over the W and WR portion of the signals to denote low signals)





The lower half of the decoder is selected when A4 is low and an input or output instruction is executed at the address set on the DIP switches. The enable for the lower half of the decoder is delayed until PWR* or PDBIN by ANDing the output from pin 6 of U110 and BIOSEL.

Serial I/O Channels 1 and 2

Ull6 and Ull7 are 2661-2 Enhanced Programmable Communication Interface (EPCI) chips. They are capable of asynchronous and synchronous data communication. Both chips convert 8-bit parallel data into serial data or vice versa.

U121, U124 and U131 are EIA TTL to RS-232 level converters. They convert the serial data (transmitted by the EPCI's) from TTL to RS-232 levels.

U122, U123 and U125 are RS-232 to TTL level converters.

The EPCI's are capable of interrupt-driven operation. When the receiver holding register has a character available, it signals the processor by pulling the RXRDY line low. This line is then used to interrupt the processor.

The EPCI's are double-buffered, which permits the processor to load another character into the EPCI while the transmitter is transmitting. When the EPCI is ready to receive a character from the processor, it pulls the TXEMPTY line low. This line is then used to interrupt the processor, which loads the next character into the chip. The EPCI can also be used in the polled mode.

Channels 1 and 2 can be configured to several modes of operation. Refer to "Detailed Configuration" discussed earlier for the settings required.

Serial I/O Channels 3 and 4

Ull8 is an Intel 8274 (or NEC 7201) Multi-Protocol Serial Communication (MPSC) chip. It is capable of asynchronous, byte synchronous and bit synchronous operation. It has two independent full-duplex transmitters and receivers. It is IBM bisync compatible. The SDLC and HDLC protocols are supported and it is also CCITT X .25 compatible.

U119 and U120 are dual Baud Rate Generators (BRG). These chips provide the transmit and receive clocks for the MPSC. The baud rate generators are programmable in software for baud rate selection. The lower four bits of the data bus are used to program the transmit clock section of the BRG's.

U139 is a 4.9512 MHz crystal, which furnishes the clock for the 2661-2 (U116 and U117) and 1943-03 (U119 and U120) baud rate generators.

The serial data output or input of the MPSC is converted to TTL or RS-232, as required, by level converters.

Serial I/O Channel 3 can be configured as shown in "Detailed Configuration" discussed earlier. Channel 4 is a limited RS-232 asynchronous port.

Parallel Input and Parallel Output

U135 (8255) is a Programmable Peripheral Interface (PPI) chip. Port A is used as an output port. Port B is used as an input port. Port C is used for control and handshaking. U136, U137 and U138 (74LS244's) buffer the data lines to the 8255. Ports A and B can be operated in either mode 0 or mode 1.

When you are using port B in mode 1 and in order to support the ring detect, connect the input strobe line to the CS line, using jumper J104. In mode 1, the PPI requires an input strobe. Without this strobe, it cannot input data.

The parallel input port is used for sensing ring detect from the RS-232 ports. Bit 1 on the parallel input port is used for sensing ring detect on RS-232 Channel 1 (P102). Bit 2 is used for sensing ring detect on RS-232 Channel 2 (P103). Bit 3 provides this function for Channel 3 (P104) and bit 4 carries Data Set Read (DSR) signal. The other 4 bits are available for other parallel input data.

Interrupt Control

Ull2 (8259) is an interrupt controller. The interrupt lines from the serial comm chips and the parallel I/O chip are connected to the IRO through IR7 lines of the interrupt controller.

Line	Function	Line	Function
IR0	RXRDY0	IR4	8255 Input Int
IR1	RXRDY1	IR5	8255 Output Int
IR2	TXRDY0	IR6	8274 Interrupt
IR3	TXRDY1	IR7	Tied to Ground

When any of these lines goes high, the INT line (pin 17 on U112) goes high. U111 inverts this signal, which is then used to turn on tri-state buffer U133. Pin 3 of U133 then goes low, driving the selected VIO* through VI7* line low to interrupt the processor.

The 8259 (U112) does not respond to the interrupt acknowledge sequence generated by the CPU. It is completely software controllable.

In the 8085 mode of the 8259, three INTA signals have to be given by software. The 8088 mode of the 8259 requires two INTA signals. Note that these modes of the 8259 are independent of the current active processor on the motherboard.

The INTA signal is generated in software by performing an input instruction from the port at Base Address + 10h, typically 070h. During the interrupt acknowledge cycle, the 8259 (U112) puts out a vector on the data bus which can be used by software to vector an interrupt service routine.

The 8259 can be selected to generate interrupts in the level-triggered mode or the edgetriggered mode. It can also be programmed to mask off unwanted interrupts, to allow polling, or to disable unused channels.

Wait State Generator

Zero, one, or two wait states can be selected, using jumper J103. If no wait states are selected, the output of pin 11 on U108 will be high. As a result, the PRDY* will be high and no additional wait states will be generated.

If the jumper on J103 is set to select one wait state, U113A remains cleared for the first S-100 bus cycle. The output from U113A (pin 5) is then inverted and goes to U108, where it is gated with BIOSEL. This generates a wait state <u>only</u> when an input or output instruction is executed. The output from U108 goes low and turns on buffer U133. The buffer output is connected to the PRDY* line, which goes low and informs the processor that a wait state is needed. The PRDY* output is sampled by the processor on the positive going edge of bus state 2.

If two wait states are required, the output of U113B stays low for two bus cycles and PRDY* is low for two bus cycles.

Note: When you use the card with an $\rm H/Z-100$ Computer, the computer automatically inserts one wait state when it is performing an I/O instruction. Programming the card for one wait state, in this case, does not add an additional wait state.

Z-204 I/O Port Pinouts

I found no information on the cables used with the Z204 Multiport I/O Card Manual, except part numbers, which is no longer helpful.

So I did a bit of research to find the following information, that you may find helpful enough to get you started with the cables.

Serial Port RS-232 DB-25 Pin Definitions

Pin	Description			
1	GND	- Protective Ground		
2	TxD	- Transmitted Data		
3	RxD	- Received Data		
4	RTS	- Request to Send		
5	CTS	- Clear to Send		
6	DSR	- Data Set Ready		
7	SG	- Signal Ground		
8	DCD	- Data Carrier Detect or		
		- Received Line Signal Detector		
9		(Reserved for dataset testing, + Voltage)		
10		(Reserved for dataset testing, - Voltage)		
11		- Unassigned		
12	DCD2	- Secondary Data Carrier Detect or		
		- Received Line Signal Detector		
13	CTS2	- Secondary Clear to Send		
14	TxD2	- Secondary Transmitted Data		
15	Tx-CLK	- DCE Transmitter Signal Element Timing		
16	RxD2	- Secondary Received Data		
17	Rx-CLK	- DCE Receiver Signal Element Timing		
18		Unassigned (Local Loopback)		
19	RTS2	- Secondary Request to Send		
20	DTR	- Data Terminal Ready		
21		- Signal Qual Detector (Remote Loopback)		
22	RI	- Ring Indicator		
23		- Data Signal Rate Selection (DTE/DCE)		
24	Tx-CLK	- DTE Transmitter Signal Element Timing		
25		- Unassigned (Text Mode)		

Serial Port RS-232 DE-9 Pin Definitions

Pin	Descri	lption	Direction
1	CD	- Carrier Detect	In Signal from DCE
2	RD	- Receive Data	In Data from DCE
3	TD	- Transmit Data	Out Data to DCE
4	DTR	- Data Term Ready	Out Handshake Signal
5	GND	- Signal Ground	Common Ref Voltage
6	DSR	- Data Set Ready	In Handshake Signal
7	RTS	- Ready to Send	Out Flow Control
8	CTS	- Clear to Send	In Flow Control
9	RI	- Ring Indicator	In Signal From DCE

Control Signals

The Control Signals are used to control flow of data between the two nodes in an RS-232 system. This gives a higher layer of control beyond what can be done in the physical layer alone and allows for a more directed focus on implementing the firmware for RS-232 systems. There are 2 to 6 common control signals that are used for handshaking between two nodes before data transmission occurs.

In applications that require some handshaking, a common use case is to use the two data signals + two control signals. These control signals are

Ready to Send (RTS) and Clear to Send (CTS). The RTS signal is asserted when the DTE has data that is ready to transmit to the DCE through the TD signal; while the CTS signal is asserted after the RTS signal has been received and the peripheral is letting the host know it is ready to receive data. However, this simple version of handshaking is not the only common handshaking signal used when using RS-232 and systems such as modems.

Modems typically add an additional 4 control signals on top of RTS and CTS. Along with RTS and CTS, common control signals also include Data Terminal Ready (DTR), Data Set Ready (DSR), Data Carrier Detect (DCD), and Ring Indicator (RI).

The DTR signal is asserted by the DTE to the DCE that it is ready to transmit or receive data while the DSR signal is asserted by the DCE to the DTE after the DTR signal to let the DTE know that it is connected to the communications line.

The DCD signal is a signal from the DCE to DTE to show that there is a valid connection between the DTE and the DCE.

Finally, the RI signal is a signal from the DCE sent to the DTE to show that there is a ringing on the communication line - or more simply that the DCE wants to communicate with the DTE itself - by which the DTE responds by asserting the DTR signal.

z-20)4 DTE		
P102		Signal	Port
Conne	ector	Direction	DB25
Pin:	Signal:	In/Out:	Pin:
1	Ground	<>	1 & 7
2		(unused)	?
3	RXD	<	3
4		(unused)	?
5	TXD	>	2
6			
7	/CTS - low	<	5
8	RDO & RI	<	22
9	/RTS - low	>	4
10			
11	/DTR - low	>	20
12	/DCD - low	<	8
13			
14	/DSR - low	<	6
15			

Z-204 DCE

P103		Signal	Port
Conne	ector	Direction	DB25
Pin:	Signal:	In/Out:	Pin:
1	Ground	<>	1 & 7
2			
3	RXD	<	3
4	DSR	<	6
5	TXD	>	2
6	DCD via J135	<	5?
7	DCD via J136	<	5?
8	RD1 & RI	<	22
9	/RTS - low	>	4
10			
11	/DTR - low	>	20
12	/DCD - low	<	8
13			
14			
15			

Z-204 DTE

P104		Signal	Port
Conne	ctor	Direction	DB25
Pin:	Signal:	In/Out:	Pin:
1	Ground	<>	1 & 7
2	RXC	< - >	17
3	RXD	<	3
4	TXC	< - >	15
5	TXD A	>	2
6			
7	/CTS A - low	<	5
8	CDB	<	22
9	/RTS A - low	>	4
10			
11	/DTR A - low	>	20
12	/CDA - low	<	8
13			
14	DSR	<	6
15			

Z-204 DCE

P105		Signal	Port
Conne	ector	Direction	DB25
Pin:	Signal:	In/Out:	Pin:
1	Ground	<>	1 & 7
2	RXC	< - >	17
3	RXD	<	3
4			
5	TXD B	>	2
6			
7			
8			
9	/RTS B - low	>	4
10			
11	/DTR B - low	>	20
12	+ 5Vdc		8?
13			
14			
15			

P104 uses the Intel 8274 Multi-protocol Serial Controller that has several unique features and signals, defined here:

8274

Symbol	Pin#	Type	Description
AO	25	I	Address selects ChA or B
			during data txfers
A1	24	I	Address selects data or
			command during transfers
/CDa	3	I	Carrier Detect (ChA)
/CDb	5	I	Carrier Detect (ChB)
/CS	23	I	Chip Select enables RD or WR
/CTSa	39	I	Clear to Send (ChA)
/CTSb	6	I	Clear to Send (ChB)
DTRa	31	0	Data Terminal Ready (ChA)
/DTRb	26	0	Data Terminal Ready (ChB)
/INT	28	0	Interrupt Signal in
/INTA	27	I	Interrupt Acknowledge
IPI &	29	I/O	Interrupt Priority In
T DO 6	30	0	Interrupt Priority Out
IΓΟ α	50	0	and TyDROb
/RD	22	т	Read controls a data byte
, 10		-	or status byte
RDYa &	32	0	Ready Transmit Data & RxDROa
RDYb &	11	0	Ready Transmit Data & TxDRQa
/RTSa	38	0	Request to Send (ChA)
/RTSb	10	I/O	Request to Send (ChB)
/RxCa	35	I	Receiver Clock (ChA) clocks
/RxCh	4	т	Receiver Clock (ChB) clocks
, 10102	-	-	in data from RxDb pin
/RxDa	34	I	Receive Data (ChA)
/RxDb	9	I	Receive Data (ChB)
RxDRQa	32	0	Synchronous DMA Data
			Transfer (ChA)
RxDRQb	29	I/O	Synchronous DMA Data
			Transfer (ChB)
/SYNDE1	33	I/O	Synchronous Detection (ChA)
/SYNDE1	10	I/O	Synchronous Detection (ChB)
			And RTSb
TxDRQa	11	0	Synchronous DMA Data
			Transfer (ChA)
TxDRQb	30	0	Synchronous DMA Data
			Transfer (ChA)
/TxCa	36	I	Transmit Clock (ChA)
/TxCb	7	I	Transmit Clock (ChB)
TxDa	37	0	Transmit Data (ChA)
TxDb	8	0	Transmit Data (ChB)
WR	21	I	Write controls transfer
			of data or commands

Note from HyperACCESS Manual Regarding Z-100 AUTODIAL Problem:

To understand the purpose of the modem adapter supplied with the Z-100 version of HyperACCESS, you need to understand the problem it overcomes - a trait singular to a Z-100's communications hardware, that makes it difficult to command an autodial modem to dial.

Ideally, when you type commands to your autodial modem to make it dial, both the commands and your modem's responses to the commands should display on your screen. But a Z-100 (unlike other computers) won't display them, or anything that comes from the modem, until the modem indicates that it has connected with a remote system.

To be more precise, the Z-100 blocks out data when an external device is applying a logiclevel low to pin 8 on the J2 port (on the J1 port, pin 20 has the same effect), and a modem normally applies a logic-level low to this pin until it connects with a remote system. Only when there is a logic-level high (or no signal at all), will the Z-100 admit data.

The modem adapter solves this by modifying the connection to the modem so no signal is applied to pin 8 on your computer's J2 connector; the adapter applies the signal that did go to pin 8, to pin 6, instead. This can not damage anything and it will have no adverse effects on performance of your computer.

If you attempt to use a modem with HyperACCESS without using this cable adapter, a number of HyperACCESS features will be inoperable, including functions on the Answer menu and the Call menu, and the connect clock in the lower right-hand corner of your screen.

Note: You may find that other modem programs do not operate correctly when the cable adapter is installed; remove the cable adapter when using such programs.

Parallel Port Pin Definitions

Pin	Description	Function
1	STROBE	A pulse that clocks data
2	PDATA1	Data to the peripheral
3	PDATA2	Data to the peripheral
4	PDATA3	Data to the peripheral
5	PDATA4	Data to the peripheral
6	PDATA5	Data to the peripheral
7	PDATA6	Data to the peripheral
8	PDATA7	Data to the peripheral
9	PDATA8	Data to the peripheral
10	ACKNLG	Acknowledge signal, fm prntr
11	BUSY	Printer Not Ready
		when signal is high
12	GND	Ground
15	ERROR	Error Signal fm prntr when low
16	INIT	Pulse Signal, Initial printer
17	GND	Ground
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground
25	GND	Ground

Centronics Parallel Port Pin Definitions

Finally, most parallel printers now use a 36-pin Centronics Connector. This pinout is usually defined as:

Pin	Descrip	oti	lon	<u>Function</u>
1	/STB	-	Low,In	STROBE pulse that
				clocks data
2	PDATA1	-	In	Data to the peripheral
3	PDATA2	-	In	Data to the peripheral
4	PDATA3	-	In	Data to the peripheral
5	PDATA4	-	In	Data to the peripheral
6	PDATA5	-	In	Data to the peripheral
7	PDATA6	-	In	Data to the peripheral
8	PDATA7	-	In	Data to the peripheral
9	PDATA8	-	In	Data to the peripheral
10	/ACK	-	Low,Out	Acknowledge signal,
				from printer
11	BUSY	-	Out	Printer Not Ready
				when signal is high
12	PO	-	Out	Paper Out
13	SLCT	-	Out	Select
14	/AFXT	-	Low,In	Autofeed Paper
15				
16	SG			Signal Ground
17	FG			Frame Ground
18	+5Vdc	-	Out	Power out from Printer
19	TWGND1			SGround - STB
20	TWGND2			SGround - DATA1
21	TWGND3			SGround - DATA2
22	TWGND4			SGround - DATA3
23	TWGND5			SGround - DATA4
24	TWGND6			SGround - DATA5
25	TWGND7			SGround - DATA6
26	TWGND8			SGround - DATA7

27	TWGND9	SGround - DATA8
28	TWGND10	SGround - ACK
29	TWGND11	SGround - BUSY
30	TWGND31	SGround - INIT
31	/INIT - Low,In	Initialize
32	/ERROR - Low,Out	Error
33	SG	Signal Ground
34		
35		
36		

TWGND## = Twisted Pair Signal Ground for pin ##.

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Para	llel OUT	Signal	Port	
P106	Connector	Direction	DB25	
Pin:	Signal:	In/Out:	Pin:	
1	STROBE	>	1	
2	PAO	>	2	
3	PA1	>	3	
4	PA2	>	4	
5	PA3	>	5	
6	PA4	>	6	
7	PA5	>	7	
8	PA6	>	8	
9	PA7	>	9	
10	/ACKa	<	10	
11				
12				
13				
14				
15	/OBFa	>	11 (BUSY)?	
16				
17				
18				
19	FGND	<>	17	
20				
21				
22				
23				
24				

z-204

25 26

Para	llel IN	Signal	Port
P107	Connector	Direction	DB25
Pin:	Signal:	In/Out:	Pin:
1	/IBFb	>	1
2	PB0	>	2
3	PB1	>	3
4	PB2	>	4
5	PB3	>	5
6	PB4	>	6
7	PB5	>	7
8	PB6	>	8
9	PB7	>	9
10	/STROBE	<	10
11			
12			

13			
14			
15	/ACKb	>	11?
16			
17			
18			
19	FGND	<>	17
20			
21			
22			
23			
24			
25			

26

Where:

/ACKa = Acknowledge Input; A "low" on this input informs the 8255A that the data from port A has been acknowledged.

/OBFa = Output Buffer Full; The OBF output will go "low" to indicate that the CPU has written data out to the specified port.

/IBFa = Input Buffer Full; The IBF input will go
"high" to indicate the data has been loaded into
the input latch.

STROBE = A "low" on this input loads data into the input latch.

Note: The pinout of the two parallel ports must be the same, as both cables are identical.

In Case of Difficulty

If your Multiport Input/Output Card is not operating properly, first check your jumper and switch settings to make sure they are configured properly.

Note: All ZDS computer hardware and software products were designed to work together as a complete system. Proper operation can be assured only when your Multiport I/O Card is used with ZDS designed or approved equipment.

The following procedures are from Chapter 8 of the Z-204 Multiport I/O Card Service Manual:

Quick Checks

Before you begin servicing, isolate the computer from all peripheral devices, such as printers, etc.

 $[\]$ Check DIP switch SW102 to be sure it is set to 060h.

[] Complete a visual inspection of the component side of the Z-204 board, looking for damaged components, bent (either out or under) integrated circuit pins, evidence of overheated components, chipped or broken components, etc. Note: A quick look along a row of IC pins while reflecting a light across them will quickly show any out of alignment with the others.

[] Complete a visual inspection of the solder side of the Z-204 board, looking for scrapes that may have damaged a trace, unsoldered pins or cold (weird looking or cracked) solder joints, etc.

[] After recording all the jumper positions of the card as received, reposition the jumper settings per the Typical Configuration.

 $\left[\right]$ Insert the Z-204 Card securely in the S-100 Bus socket.

[] Connect all cables to the Z-204 Card

[] Connect all cables removed from other cards during 'Disassembly'.

[] Connect computer line cord to an AC receptacle.

Z-204 Test

Testing the Z-204 Card consists of four steps: Addressing, Continuous Output (Channel 1), Echo (Channel 1), and Interrupt for all 4 Channels. Do not proceed from one test to the next until the card has passed each of these tests.

When you are running these tests, use the following procedure:

- Test each card separately.

- After the first card has passed all the tests, remove it from the S-100 slot and install the next Z-204 Card to be tested.

- Be sure DIP switches and jumpers are in their correct positions **on each card**.

- Turn on your computer and, using the CP/M-85 Operating System, perform the following steps:

Addressing Test

[] Insert your system disk into the drive and boot up your computer.

[] At the prompt, enter the following commands exactly as shown:

A> ddt		{RETURN}
DDT VERS	2.2	{RETURN}
A100		{RETURN}

[] Type in the following program at location 100h:

0100	MVI A,00	{RETURN]
0102	OUT 60	{RETURN }
0107	JMP 100	{RETURN }

[] Press the {**RETURN**} key a second time.

After you enter the above program and pressed return, the DDT prompt should be on the screen.

[] Type in: G100 {RETURN}

At this point, you should see LED D101 dimly lit. If you have an oscilloscope, place your probe on pin 10 of U111. A number of pulses should be visible. If there is NO activity on this line and D101 is NOT flickering, your card is not being selected and further debugging needs to be done. Refer to the Symptoms and Checks, Table 5, following this section.

Note: Be sure your I/O card passes this addressing test BEFORE you start any of the following tests; to proceed would be pointless.

Continuous Output Test for Channel 1

The purpose of this test is to see whether the serial I/O channel output on the card is functioning properly under the polled mode operation. To perform this test, connect an additional terminal to your computer.

[] Using the CP/M-85 Operating System, reboot the system;

$\{CTRL\} - \{RESET\} \ \{B\} \text{oot}$

Then, enter the following program using DDT at memory location 100h.

Or, if you would rather not use DDT, type in the program using a standard CP/M editor. Then, assemble and load this new program:

A>DDT			{RETURN}
DDT V	YERS 2	.2	{RETURN}
A100			{RETURN}
0100	MVI	A,4E	{RETURN}
0102	OUT	62	{RETURN}
0104	MVI	A,76	{RETURN}
0106	OUT	62	{RETURN}
0108	MVI	A,27	{RETURN}
010A	OUT	63	{RETURN}
010C	MVI	A,41	{RETURN}
010E	OUT	60	{RETURN}
0110	IN	61	{RETURN}

0112	ANI	01	{RETURN}
0114	JZ	0110	{RETURN}
0117	JMP	010C	{RETURN}
011A			{RETURN} {RETURN}

 $\left[\right]$ Connect a terminal to port 1 on the I/O card.

[] Set the terminal for 300 baud full duplex and in the Online Mode.

[] Run the program by typing in:

A>G100 {RETURN}

A string of A's will be output on your CRT screen. If the test fails, refer to Symptoms and Checks, Table 5.

Echo Test for Channel 1

[] Reset and reboot CP/M-85.

[] Using the DDT utility in CP/M-85, type in the program below. This program echoes a character typed on the terminal keyboard to the terminal screen.

А	>DDT		{RETURN}	
	DDT V	ERS 2.	{RETURN}	
	A100			{RETURN}
	0100	MVI	A,4E	{RETURN}
	0102	OUT	62	{RETURN}
	0104	MVI	A,76	{RETURN}
	0106	OUT	62	{RETURN}
	0108	MVI	A,27	{RETURN}
	010A	OUT	63	{RETURN}
	010C	IN	61	{RETURN}
	010E	ANI	02	{RETURN}
	0110	JZ	010C	{RETURN}
	0113	IN	60	{RETURN}
	0115	OUT	60	{RETURN}
	0117	IN	61	{RETURN}
	0119	ANI	01	{RETURN}
	011B	JZ	0117	{RETURN}
	011E	JMP	010C	{RETURN} {RETURN}

[] Enter:

A>G100 {RETURN}

[] Type any character on the terminal and check the screen for 'echo' of the typed character.

[] Run the program. If the test fails, refer to Symptoms and Checks, Table 5.

Interrupt Test of All 4 Channels

For this test, use the H/Z-DOS operating system. If the test fails, refer to Symptoms and Checks, Table 5, next.

[] Using the setup of the previous test, type in the program TR7 from the Z-204 Multiport Input/Output Card Manual. Make sure that jumper J101A is in the ON position, enabling the VIO* interrupt.

Note: I have retyped the TR7 listing from the Z-204 Manual and have listed it here next, but it would still need the code to be entered into DEBUG or as an assembly source code document and assembled to run.

[] Connect four terminals to the four serial I/O ports. Set the terminals for 300 baud. Or, using one terminal set for 300 baud, test each port in turn. Connect an Epson printer to the parallel output port, P106.

[] Type; **TR7** {RETURN}

The following message should appear on the terminal screens.

Terminal n: "Test string n"

Where "n" is the number of the communication port.

[] Type in any character on the keyboard of a terminal. The character typed in should be echoed on the terminal screen. This indicates the card is now transmitting and receiving messages under interrupts.

[] Check the interrupt LED D102 to see if it is dim. Due to the high frequency of the interrupt signal, you will not be able to see the LED flicker.

Table 5. Symptoms and Checks

Symptoms	Che	ecks
Card fails	1.	DIP switch SW102 set to
addressing		addr 060h?
test	2.	Jumper J102 is on right
		& center pins, for
		8-bit addressing?
	З.	Check for BDSEL signal
		(inverted) out of
		U106, pin 19?
	4.	Check supply voltages?
	5.	Follow the signal paths thru
		U109, U110, & U111.
Card fails	1.	Test Pgm entered correctly?
continuous	2.	Terminal set at 300 baud?
output test	З.	Check EPCI CSO Signal on U132,
on Channel 1		pin 12.
	4.	Check Clock Signal on
		U116, pin 20.
	5.	Check the TXD line on
		U116, pin 19.
	6.	Check for TXD Signal on
		U121, pin 8 & P102, pin 5.
Card fails	1.	Check for RXD Signal on
Echo Test		U122, pin 1 & P102, pin 5.
Card fails	1.	Check jumper installed on
Interrupt		J101A ONLY.
Test	2.	Jumper J111 Installed?
		Check if LED D102 glows?
	3.	Check TXRDY0 Signal on
		U111, pin 11 & U112, pin 20.
	4.	Check INT Signal on

Note: The schematic was too large to post here. It is available from the "Z-100 LifeLine" for a minimal fee for copy charges and postage.

U112, pin 17.

5. Check U112 and U132.

If you have any questions or comments, please email me at:

z100lifeline@swvagts.com

Cheers,

Steven W. Vagts



Z-204 Multiport Input/Output Card

Application Example

These programming routines will provide an example of the interrupt and echo functions of this card. Use ZDOS to enter, assemble, and save the routines on disk or use DEBUG to just enter the code in the left columns.

This program has been typed and saved from the "Zenith Z-204-RD Multiport Input/Output Card" Manual by Steven W. Vagts, "Z-100 LifeLine" using MS WordPad, Courier New, 9 pitch.

The Microsoft MACRO As TR7.ASM 8088	ssembler	10-17-83	Page 1-1
1		PAGE	,132
2	;****	* * * * * * * * * * * * *	******
3	;		
4	;	FILE: TR7.	ASM
5	;		
6	;****	* * * * * * * * * * * * *	******
7	;		
8	;	DISK: Z-10)
9	;		
10	;	Copyright (c)1983 Zenith Data Systems
11	;		
12	;****	**********	*********
13	;		
14	;	This routin	e tests out the Z-204 I/O Board using interrupts.
15	;	The softwar	e transmits a string of characters to the four
16	;	serial port	s and the printer port all under interrupt control.
17	;	The softwar	e also accepts a character typed into a
18	;	terminal an	d echoes it back to the terminal.
19	;		
20	;****	* * * * * * * * * * * * *	* * * * * * * * * * * * * * * * * * * *
21	;		
22	;	Written by	Hoshang Pestonji under the direction of
23	;	George Pisk	orz.
24	;		
25	;****	* * * * * * * * * * * * *	* * * * * * * * * * * * * * * * * * * *
26	;		
27		PAGE	
28	;****	* * * * * * * * * * * * *	* * * * * * * * * * * * * * * * * * * *
29	;		
30	;	Initializat	ion
31	;		
32	;****	* * * * * * * * * * * * *	* * * * * * * * * * * * * * * * * * * *
33	;		
34		TITLE TR7.	ASM 8088
35	;		

36		P	SSUME	CS:CSE	EG, DS:CSEG, SS:STSEG, ES:CSEG
37		;			
38	0000	CSEG S	EGMENT		
39		;			
40	0000	INIT:			
41		;			
42	0000 B8 R	Μ	IOV AX, DSI	EG	
43	0003 8E D8	Μ	IOV DS,AX		
44		;			
45	0005 EB 08 90	J	MP INIT1		
46		;			
47	0008 54 52 37 2E 43	153 E	B 'TR7.	ASM'	
48	4 D				
49		;			
50	= 0060	SERIAL I	I O ADRS	EQU	060h ; Address of EPCI 0
51		; –			_
52	= 0070	VIO ADRS	5	EQU	SERIAL I O ADRS+010h
53		;			
54	= 0078	PAR I O	ADRS	EQU	SERIAL I O ADRS+018h ; Addr of Parallel I/O
55		;	_		
56	= 007C	DATA_POR	RT_CHA	EQU	VI0_ADRS+0Ch ; 8274 Channel A Data Port
57		;			
58	= 007D DATA P		RT_CHB	EQU	VI0_ADRS+0Dh ; 8274 Channel B Data Port
59		;			
60	= 007E	COM_POR	Г_СНА	EQU	VI0_ADRS+0Eh ; Channel A Command Port
61		;			
62	= 007F	COM_POR	Г_СНВ	EQU	VI0_ADRS+0Fh ; Channel B Command Port
63		;			
64		;*****	* * * * * * * * * * * *	******	******
65		;			
66		; I	nitialize E	PCI	
67		;			
68		;*****	* * * * * * * * * * * * *	******	******
69	= 004E	Μ	IR1_0	EQU	04EH
70		;			
71	= 0076	Μ	IR2_0	EQU	076h
72		;			
73	= 0027	C	CR1_0	EQU	027h
74		;			
75	000F	INIT1:			
76	000F FA	C	LI		
77			PAGE		
78		;******	* * * * * * * * * * * *	******	**************
79		;			
80		; 1	nitialize P	arallel	I/O Chip
81		;			

82				;***	* * * * * * * *	* * * * * * * *	*****	* * * * * * * * * * * * * * * * * * * *
83				;				
84	= 000)B		STRO	BEON		EQU	00001011b
85	= 000	A(STRO	BEOFF		EQU	00001010b
86				;				
87	0010	в0	A6		MOV	AL,101	1001101	b
88				;				
89	0012	BA	007B			MOV	DX,PA	AR_I_O_ADRS+03h ; 8255 Control Por
90	0015	ΕE			OUT	DX,AL		
91				;				
92	0016	в0	0B		MOV	AL,STI	ROBEON	; Set PC5
93	0018	BA	007B		MOV	DX,PAI	r_i_o_ <i>i</i>	ADRS+03h
94	001B	ΕE			OUT	DX,AL		
95				;				
96				;***	* * * * * * * *	* * * * * * * *	*****	* * * * * * * * * * * * * * * * * * * *
97				;				
98				;	Initi	alize E	PCI_0	
99				;				
100				;***	* * * * * * * *	* * * * * * * *	*****	*********
101				;				
102	001C	ΒA	0062		MOV	DX,SEH	RIAL_I_	_O_ADRS+02h ;Port 0 Address
103	001F	в0	4E		MOV	AL,MR	1_0	
104	0021	ΕE			OUT	DX,AL		
105	0022	в0	76		MOV	AL,MR2	2_0	
106	0024	ΕE			OUT	DX,AL		
107				;				
108	0025	83	C2 01		ADD	DX , 1		
109	0028	в0	27		MOV	AX,CR	1_0	
110	002A	ΕE			OUT	DX,AL		
111				;				
112				;***	* * * * * * * *	* * * * * * * *	*****	*********
113				;				
114				;	Initi	alize E	PCI_1	
115				;				
116				;***	* * * * * * * *	* * * * * * * *	*****	*********
117				;				
118	002B	ΒA	0066		MOV	DX,SEH	RIAL_I	_O_ADRS+06h
119	002E	в0	4E		MOV	AL,MR1	1_0	
120	0030	ΕE			OUT	DX,AL		
121	0031	в0	76		MOV	AL,MR2	2_0	
122	0033	ΕE			OUT	DX,AL		
123	0034	83	C2 01		ADD	DX,1		
124	0037	в0	27		MOV	AL,CR	1_0	
125	0039	ΕE			OUT	DX,AL	-	
126				;				
127						PAGE		

128			;******* ;	*****	* * * * * * * * * * * * *	*****
129			;			
130			; In	itialize 8274	MPSC	
131			;			
132			;*******	****	* * * * * * * * * * * * *	*****
133			; Ch	annel_A Initi	alization	
134			;*******		* * * * * * * * * * * * *	*****
135	003A	в0 55	MO	V AL,055h		; CH_A Baud Rate = 300
136	003C	BA 0068	MO	V DX,SERIA	L_I_O_ADRS+0	Bh
137	003F	EE	OU	T DX,AL		; Baud Rate
138			;			
139	0040	в0 55	MO	V AL,055h		; CH_B Baud Rate = 300
140	0042	BA 006C	MO	V DX,SERIA	L I O ADRS+00	 Ch
141	0045	EE	OU	T DX,AL		
142			;			
143	0046	BA 007E	MO	V DX,COM P	ORT CHA	
144	0049	в0 18	MO	V AL,18h	—	
145	004B	EE	OU	T DX,AL		; Output channel reset A
146			; * * * * * * * * *	****	* * * * * * * * * * * * *	
147	004C	B1 04	MO	V CL,04h		
148	004E	E2 FE	DELAY1:	LOOP D	ELAY1	; Delay loop
149			;			
150	0050	в0 02	MO	V AL,02h		
151	0052	EE	OU	T DX,AL		; Set pointer to command reg 2
152	0053	в0 14	MO	V AL,00010	100b	
153	0055	EE	OU	T DX,AL		; Output command word
154			;			-
155	0056	в0 04	МО	V AL,04h		; Set command reg pointer to 4
156	0058	EE	OU	T DX,AL		
157	0059	в0 44	МО	V AL,44h		; Output command word
158	005B	EE	OU	T DX,AL		-
159			;			
160	005C	в0 01	МО	V AL,01h		
161	005E	EE	OU	T DX,AL		
162	005F	B0 1A	МО	V AL,00011	010b	; Write to command reg 1
163	0061	EE	OU	T DX,AL		5
164			;			
165	0062	в0 05	MO	V AL,05h		
166	0064	EE	OU	T DX,AL		
167	0065	BO EA	МО	V AL,11101	010b	
168	0067	EE	OU	T DX,AL		; Write to command reg 5
169			;	,		
170	0068	B0 03	MO	V AL.03h		
171	006A	EE	011	T DX, AT,		
- 172	006B	B0 E1	MO	V AL.11100	001b	
173	006D	EE	011	T DX.AT.		
			00	,		

174				;									
175						PAGE							
176				;****	******	******	* * * * * * * * * * *	*****	* * * * * *	***	******	:****	· *
177				;	Chann	el_B Ini	itializatio	n					
178				;****	******	*******	******	*****	* * * * * *	***	******	:****	· *
179	006E	B0 18			MOV	AL,018	h						
180	0070	BA 007F			MOV	DX,COM	I PORT CHB						
181	0073	EE			OUT	DX,AL		;	Channe	el E	3 reset		
182				;									
183	0074	B1 04			MOV	CL,04h	1						
184	0076	E2 FE		DELAY	2:	LOOP	DELAY2	;	Delay	loc	op for 82	274	
185				;					1		-		
186	0078	B0 04			MOV	AL,04h	1						
187	007A	BA 007F			MOV	DX,COM	1 PORT CHB						
188	007D	EE			OUT	DX,AL		;	Point	to	command	req	4
189	007E	B0 44			MOV	AL,010	00100b					5	
190	0080	EE			OUT	DX,AL		;	Write	to	command	req	4
191				;		·						5	
192	0081	B0 01			MOV	AL,01h	1						
193	0083	EE			OUT	DX,AL		;	Point	to	command	req	1
194	0084	B0 1E			MOV	, AL,000)11110b					2	
195	0086	EE			OUT	DX,AL		;	Write	to	command	req	1
196				;								2	
197	0087	B0 03			MOV	AL,03h	1						
198	0089	EE			OUT	DX,AL		;	Point	to	command	req	3
199	008A	B0 E1			MOV	AL,111	.00001b					5	
200	008C	EE			OUT	DX,AL		;	Write	to	command	req	3
201				;								2	
202	008D	B0 05			MOV	AL,05h	1						
203	008F	EE			OUT	DX,AL		;	Point	to	command	reg	5
204	0090	B0 EA			MOV	AL,111	01010b					2	
205	0092	EE			OUT	DX,AL		;	Write	to	command	reg	5
206				;		·						5	
207						PAGE							
208				;****	******	******	* * * * * * * * * * *	*****	* * * * * *	***	******	****	: *
209				;	Set u	p Interi	rupt Vector	Loca	tion				
210				;		-	-						
211				;****	******	******	* * * * * * * * * * *	*****	* * * * * *	***	******	****	: *
212				;									
213	0093	B8 016E	R		MOV	AX,off	set VIO SEI	RVICE					
214				;			_						
215	0096	в9 0000			MOV	CX,0							
216	0099	8E C1			MOV	ES,CX							
217	009B	8C C9			MOV	CX,CS							
218	009D	BB 0060			MOV	BX,006	50h						
219	00A0	26: 89	07		MOV	ES:[E	X],AX						

220	00A3	83	C3 02		ADD	BX,2
221	00A6	26	89 OF		MOV	ES:[BX],CX
222				;		
223				;		
224				;****	******	*************
225				;		
226				;	Initi	alize Serial I/O Int Generator
227				;		
228				;****	******	****************
229	00A9	BA	0074		MOV	DX,SERIAL_I_O_ADRS+014h
230	00AC	в0	13		MOV	AL,013h
231	00AE	ΕE			OUT	DX,AL
232				;		
233	00AF	BA	0075		MOV	DX,SSERIAL_I_O_ADRS+015h
234	00B2	в0	00		MOV	AL,00h
235	00B4	ΕE			OUT	DX,AL
236				;		
237	00B5	в0	01		MOV	AL,01h
238	00B7	ΕE			OUT	DX,AL
239				;		
240						PAGE
241				;****	******	***************************************
242				;		
243				;	Initi	alize the Master Interrupt Generator
244				;		
245				;****	******	***************************************
246	00B8	ΒA	00F3		MOV	DX,0F3h
247	00BB	в0	FF		MOV	AL, OFFh
248	00BD	ΕE			OUT	DX,AL
249				;		
250	00BE	ΒA	00F2		MOV	DX,oF2h
251	00C1	в0	AO		MOV	AL,10100000b
252	00C3	ΕE			OUT	DX,AL
253				;		
254				;		
255	00C4	ΒA	00F2		MOV	DX,0F2h
256	00C7	в0	15		MOV	AL,00010101b
257	00C9	ΕE			OUT	DX,AL
258				;		
259	00CA	BA	00F3		MOV	DX,0F3h
260	00CD	в0	00		MOV	AL,00h
261	OOCF	ΕE			OUT	DX,AL
262				;		
263	00D0	в0	08		MOV	AL,00001000b
264	00D2	ΕE			OUT	DX,AL
265				;		

266	00D3	в0	01		MOV	AL,0000001b	
267	00D5	ΕE			OUT	DX,AL	
268	3			;			
269)			;			
270)			;****	* * * * * * *	*****	* * * * * * * * * * * * * * * * * * * *
271				;			
272)			;	Initia	lize the Slave Inter	crupt Generator
273	3			;			
274	ł			;****	* * * * * * *	*****	* * * * * * * * * * * * * * * * * * * *
275	5			;			
276	00D6	BA	00F0		MOV	DX,0F0h	
277	00D9	в0	1D		MOV	AL,00011101b	
278	8 00D8	ΕE			OUT	DX,AL	
279)			;			
280	00DC	ΒA	00F1		MOV	DX,0F1h	
281	. 00DF	в0	18		MOV	AL,00011000b	
282	2 00E1	ΕE			OUT	DX,AL	
283	}			;			
284	00E2	в0	03		MOV	AL,00000011b	
285	00E4	ΕE			OUT	DX,AL	
286	-)			;			
287	00E5	в0	01		MOV	AL,0000001b	
288	00E7	ΕE			OUT	DX,AL	
289)			;			
290)					PAGE	
291				;****	* * * * * * *	****	******
292	2			;	Start	Outputting messages	to devices
293	3			;****	* * * * * * *	****	******
294	l			;			
295	00E8	BF	00C9 R		MOV	DI, offset PRNT_STRI	NG ; Get start address of
296	00EB	ΒA	05		MOV	AL,[DI]	; string and get char
297	00ED	ΒA	0078		MOV	DX,PAR_I_O_ADRS	
298	00F0	ΕE			OUT	DX,AL	; Output first char of
299)						; print string to printer
300	00F1	47			INC	DI	; Setup printer to next char
301	. 00F2	89	3E 0101 R		MOV	POINTER_4,DI	
302	2 00F6	83	C2 03		ADD	DX,3	
303	00F9	в0	0A		MOV	AL,STROBEOFF	
304	00FB	ΕE			OUT	DX,AL	; Generate print strobe
305	00FC	в0	0B		MOV	AL, STROBEON	; to printer
306	00FE	ΕE			OUT	DX,AL	
307	1			;			
308	8 00FF	В8	0000 R		MOV	AX, offset STRING 0	; Get start address of
309	0102	A3	00F9 R		MOV	POINTER 0,AX	; print string 0
310)			;		—	
311	0105	В8	0031 R		MOV	AX,offset STRING_1	; Get start address of

312	0108	A3	00FB R		MOV	POINTER_1,AX	; print string 1
313				;			
314				;			
315	010B	8B	1E 00F9 R		MOV	BX, POINTER_0	
316	010F	8A	07		MOV	AL,[BX]	; Get first char of string 0
317	0111	BA	0060		MOV	DX,SERIAL_I_O_ADRS	; and output it to terminal
318	0114	ΕE			OUT	DX,AL	; one
319	0115	43			INC	BX	; Increment pointer by one
320	0116	89	1E 00F9 R		MOV	POINTER_0,BX	; and save it
321				;			
322	011A	8B	1E 00FB R		MOV	BX, POINTER_1	
323	011E	8A	07		MOV	AL,[BX]	; Get first char of string 0
324	0120	BA	0064		MOV	DX,SERIAL_I_O_ADRS+0	04h ; & output it to terminal
325	0123	ΕE			OUT	DX,AL	; one
326	0124	43			INC	BX	; Increment pointer by one
327	0125	89	1E 00FB R		MOV	POINTER_1, BX	; and save it
328				;			
329	0129	В8	0064 R		MOV	AX,offset STRING_2	; Get addr of first char
330	012C	A3	00FD R		MOV	POINTER_2,AX	; in string 2
331	012F	8B	3E 00FD R		MOV	DI, POINTER_2	
332	0133	8A	05		MOV	AL,[DI]	; Get first char in string
333	0135	BA	007C		MOV	DX,DATA_PORT_CHA	; and output it
334	0138	ΕE			OUT	DX,AL	
335	0139	47			INC	DI	
336	013A	89	3E 00FD R		MOV	POINTER_2,DI	; Point to next char
337				;			
338	013E	В8	0096 R		MOV	AX,offset STRING_3	; Get addr of first char
339	0141	A3	00FF R		MOV	POINTER_3,AX	; in string 2
340	0144	8B	3E OOFF R		MOV	DI, POINTER_3	
341	0148	8A	05		MOV	AL,[DI]	; Get first char in string
342	014A	BA	007D		MOV	DX,DATA_PORT_CHB	; and output it
343	014D	ΕE			OUT	DX,AL	
344	014E	47			INC	DI	
345	014F	89	3E OOFF R		MOV	POINTER_3,DI	; Point to next char
346				;		_	
347	0153	BA	007B		MOV	DX,PAR_I_O_ADRS+03h	
348	0156	в0	0 D		MOV	AL,0Dh	
349	0158	ΕE			OUT	DX,AL	; Enable parallel intr
350				;			
351	0159	BA	0075		MOV	DX,SERIAL_I_O_ADRS+(015h
352	015C	в0	80		MOV	AL,10000000b	
353	015E	ΕE			OUT	DX,AL	; Enable Serial I/O intr
354				;			
355				;			
356	015F	BA	00F3		MOV	DX,0F3h	; Enable Master Interrupts
357	0162	в0	F7		MOV	AL,0F7h	-

358	0164	ΕE			OUT	DX,AL	
359				;			
360				;			
361	0165	BA O	0F1		MOV	DX,0F1	h ; Enable Slave Intr
362	0168	B0 F	E		MOV	AL,OFE	h
363	0164	ΕE			OUT	DX,AL	
364				;			
365	016B	FB			STI		
366				;			
367						PAGE	
368				;****	******	******	*********
369				;	Idle L	qoo	
370				;****	******	******	*********
371				;			
372	016C	EB F	E	LOOP:		JMP L	OOP
373				;			
374						PAGE	
375				;****	******	******	*******
376				;			
377				;	Interr	upt Ser	rvice Routine
378				;			
379				;****	******	******	********
380	016E			VIO_SE	RVICE:		
381				;			
382	016E	BA O	070		MOV	DX,VIO	ADRS
383	0171	EC			IN	AL,DX	; Dummy read which serves as first INTA
384							; to the 8259 on serial board
385	0172	EC			IN	AL,DX	; Second read serves as second INTA and
386							; accumulator contains interrupt vector
387							; NOTE: Instead of a hardware INTA sequence,
388							; the INTA sequence is simulated in software.
389	0173	D0 E	0		SHL	AL,1	; Multiply interrupt vector by two
390	0175	В4 О	0		MOV	AH,0	
391	0177	8B F	0		MOV	SI,AX	; Interrupt vector serves as offset into
392							; vector table
393	0179	BD 0	111 R		MOV	BP,off	set INT_VEC_TABLE ; Start address
394							; of vector table
395	017C	3E:	8B 0A		MOV	CX,DS:	[BP+SI] ; Form vector address
396							; by adding offset to
397							; starting address
398	017F	FF E	1		JMP	СХ	
399				;			
400				;****	******	******	* * * * * * * * * * * * * * * * * * * *
401				;			
402				;	Interr	upt Ser	vice routine for Receiver INT from Channel 1
403				;			

404 405 406 0181 BA 0060 RECEIVE 0: MOV DX, SERIAL I O ADRS RO BUSY: IN AL, SERIAL I O ADRS+01h ; Input from status 407 0184 E4 61 AND AL,01h ; of 2661 and check for 408 0186 24 01 ; transmit ready 409 410 0188 3C 01 CMP AL,01h 411 018A 75 F8 JNZ RO BUSY ; Continue if not busy 412 018C EC IN AL,DX ; Get character 413 018D EE OUT DX,AL ; Echo it back 414 018E EA 029D ---- R JMP FAR PTR EXIT 415 PAGE 416 ; 417 418 ; 419 Interrupt Service routine for Receiver INT from Channel 2 ; 420 421 422 0193 BA 0064 RECEIVE 1: MOV DX,SERIAL I O ADRS+04h 423 0196 E4 65 R1 BUSY: IN AL, SERIAL I O ADRS+05h ; Input status 424 0198 24 01 AND AL,01h ; and check for busy 425 019A 3C 01 CMP AL,01h 019C 75 F8 JNZ R1 BUSY 426 ; Continue if not busy IN AL,DX 427 019E EC ; Input char from terminal 428 019F EE OUT DX,AL ; Echo it back 429 01A0 EA 029D ---- R JMP FAR PTR EXIT 430 : 431 432 ; 433 ; Interrupt Service routine for Transmitter INT from CH 1 434 435 436 01A5 8B 3E 00F9 R TRANSMIT 0: MOV DI, POINTER 0 437 01A9 BA 0060 MOV DX, SERIAL I O ADRS 01AC E4 81 BUSY1: IN AL,081h 438 439 01AE 24 01 AND AL,01h ; Check for busy 440 01B0 3C 01 CMP AL,01h 01B2 75 F8 ; Continue if not busy 441 JNE BUSY1 01B4 8A 05 442 MOV AL,[DI] ; Get char from string 443 01B6 EE OUT DX,AL ; Output it to terminal 01B7 47 444 INC DI ; Point to next char MOV 01B8 89 3E 00F9 R 445 POINTER 0,DI ; Store pointer 01BC 8A 05 MOV 446 AL,[DI] 01BE 3C 00 447 CMP AL,00h ; Check for end string char JNZ EXIT1 448 01C0 75 06 449 01C2 B8 0000 R MOV AX, offset STRING 0 ; If end of string, set

450	01C5	A3 00F9 R	MOV	POINTER_0,AX	; pointer to beginning
451	01C8	EA 029D	R EXIT1:	JMP FAR PTR EXIT	
452			;		
453			• * * * * * * * * * * * * * * * * * *	******	******
454			;		
455			; Inter	rupt Service routine	for Transmitter INT from CH_2
456			;		
457			;*********	*****	******
458	01CD	8B 00FB R	TRANSMIT_1:	MOV DI, POINTER_1	
459	01D1	BA 0064		MOV DX, SERIAL_I_	O_ADRS+04h
460	01D4	8A 05	MOV	AL,[DI]	; Get character
461	01D6	EE	OUT	DX,AL	; Output it
462	01D7	47	INC	DI	; Point to next char
463	01D8	89 3E 00FB R	MOV	POINTER_1,DI	; Store pointer
464	01DC	8A 05	MOV	AL,[DI]	
465	01DE	3C 00	CMP	AL,00h	; Check for end string char
466	01E0	75 06	JNZ	EXIT2	
467	01E2	B8 0031 R	MOV	AX, offset STRING_1	; Reset pointer to
468	01E5	A3 00FB R	MOV	POINTER_1,AX	; beginning of string
469	01E8	EA 029D	R EXIT2:	JMP FAR PTR EXIT	
470			;		
471				PAGE	
472			;*********	****	*****
473			;		
474			; Inter	rupt Service routine	for input from Parallel Port
475			;		
476			;*********	****	*****
477	01ED	BA 0078	PRNT_IN:	MOV DX, PAR_I_O_A	DRS
478	01F0	EC	IN	AL,DX	; Input from Parallel port
479	01F1	BB 00C8 R	MOV	BX, offset INCHAR	
480	01F4	88 07	MOV	[BX],AL	; Store in MEM LOC
481	01F6	EB FO	JMP	EXIT2	
482			;*********	****	*****
483			;		
484			; Inter	rupt Service routine	for output from Parallel Port
485			;		
486			;**********	****	*****
487	01F8		PRNT_OUT:		
488	01F8	BA 007A	BUSY:	MOV DX, PAR_I_O_A	DRS+02h
489	01FB	EC	IN	AL,DX	
490	01FC	24 80	AND	AL,1000000b	; Busy mask
491	01FE	74 F8	JZ	BUSY	
492					
493	0200	8B 3E 0101 B	r Mov	DI,POINTER 4	
494	0204	BA 0078	MOV	DX,PAR I O ADRS	
495	0207	8A 05	MOV		; Get next char from string

496	0209	ΕE		(TUC	DX,AL		;	Output the char
497								;	to the printer
498	020A	BA C)07B	1	VON	DX,PAR_I_	O_ADRS+03h		
499	020D	в0 С)A	1	VON	AL, STROBE	OFF		
500	020F	ΕE		(TUC	DX,AL		;	Issue low going print strobe
501								;	to the printer
502									
503	0210	в0 С)B	1	VON	AL, STROBE	ON		
504	0212	ΕE		(TUC	DX,AL		;	Reset print strobe
505									
506	0213	47		-	INC	DI		;	Increment DI to print to
507								;	next char in print string
508	0214	89 3	3E 0101 R	1	VON	POINTER_4	,DI		
509	0218	8A ()5	1	VON	AL,[DI]			
510	021A	3C (00	(CMP	AL,00h		;	Check for end of string
511	021C	75 7	7 F	L.	JNZ	EXIT			
512	021E	B8 C	00C9 R	1	VON	AX,offset	PRNT_STRI	NG	
513	0221	A3 (0101 R	1	VON	POINTER_4	,AX		
514	0224	EB 7	77 90	,	JMP	EXIT		;	Initialize print string
515								;	to start of print string
516									
517						PAGE			
518				;*****	*****	*******	*********	***	******
519				;					
520				;	Interr	upt Servio	ce routine	fo	r MPSC Interrupt
521				;					
522				;*****	*****	*******	* * * * * * * * * * *	***	******
523	0227	BA C)07F	TR_8274	:	MOV DX	,COM_PORT_C	CHE	3
524	022A	B0 C)2	1	VON	AL,02h			
525	022C	ΕE		(TUC	DX,AL		;	Set pointer to Reg 2
526	022D	EC		:	IN	AL,DX		;	Read vector from Reg_2 CH_B $$
527	022E	В4 С	00	1	VON	AH,0			
528	0230	8B F	<u>7</u> 0	1	VON	SI,AX			
529	0232	BD C)11F R	1	VON	BP,offset	JMP_TABLE		
530	0235	3E:	8B 0A	1	VON	CX,DS:[BP	P+SI]	;	Form address into jump table
531	0238	FF E	51	ı	JMP	CX		;	Jump to service routine
532				;					
533				;*****	*****	******	*********	***	*******
534				;					
535				;	[ransm	it interru	upt service	e r	outine for CH_B
536				;					
537				;*****	*****	******	*********	***	******
538	023A	BA C	07D	TRANSMI	Т_СН_В	B: MO	V DX,DAT	'A_	PORT_CHB
539	023D	8B 3	BE OOFF R	1	VON	DI, POINTE	R_3		
540	0241	8A ()5	1	VON	AL,[DI]			
541	0243	ΕE		(TUC	DX,AL		;	Output char to terminal 4

542	0244	47		INC	DI		; Point to next char
543	0245	89 3E 00FF R		MOV	POINTER_3,DI		
544	0249	8A 05		MOV	AL,[DI]		
545	024B	3C 00		CMP	AL,00h		
546	024D	75 48		JNZ	EOI_COM		; Check for end of string
547	024F	B8 0096 R		MOV	AX, offset STR	RING_3	
548	0252	A3 00FF R		MOV	POINTER_3,AX		; Point to begin of string
549	0255	EB 40 90		JMP	EOI_COM		
550			;				
551			;*****	* * * * * * *	* * * * * * * * * * * * * * * *	******	*****
552			;				
553			;	Receiv	e interrupt se	ervice	routine for CH_B
554			;				
555			;*****	******	* * * * * * * * * * * * * * *	* * * * * * *	*****
556			;				
557	0258	BA 007F	RECEIV	E_CH_B:	MOV	DX,COM	_PORT_CHB
558	025B	EC	R2_BUS	Y:	IN	AL,BX	; Input status
559	025C	24 04		AND	AL,04h		
560	025E	3C 04		CMP	AL,04h		; Check for busy
561	0260	75 F9		JNZ	R2_BUSY		; Continue if not busy
562	0262	BA 007D		MOV	DX,DATA_PORT_	CHB	
563	0265	EC		IN	AL,DX		; Input char from terminal
564	0266	EE		OUT	DX,AL		; Echo it back to terminal
565	0267	EB 2E 90		JMP	EOI_COM		
566			;				
567					PAGE		
568			;*****	******	* * * * * * * * * * * * * * *	******	* * * * * * * * * * * * * * * * * * * *
569			;				
570			;	Transm	it interrupt :	service	routine for CH_A
571			;				
572			;*****	******	******	******	*****
573			;				
574	026A	BA 007C	TRANSM	IT_CH_A	A: MOV	DX,DAT	A_PORT_CHA
575	026D	8B 3E 00FD R		MOV	DI, POINTER_2		
576	0271	8A 05		MOV	AL,[DI]		; Get character
577	0273	EE		OUT	DX,AL		; Output char
578	0274	47		INC	DI		; Point to next char
579	0275	89 3E 00FD R		MOV	POINTER_2,DI		
580	0279	BA 05		MOV	AL,[DI]		
581	027B	3C 00		CMP	AL,00h		; Check for end of string
582	027D	75 18		JNZ	EOI_COM		; Exit if no end of string
583	027F	B8 0064 R		MOV	AX, offset STF	RING_2	
584	0282	A3 00FD R		MOV	POINTER_2,AX		; Point to begin of string
585	0285	EB 10 90		JMP	EOI_COM		
586			;				
587			;*****	******	* * * * * * * * * * * * * * *	* * * * * * *	*****

588			;					
589			;	Receiv	ve interrupt	service	routine for CH_B	
590			;					
591			;****	* * * * * * * *	* * * * * * * * * * * *	******	****	· * *
592			;					
593	0288	BA 007E	RECEIV	VE_CH_A	: MOV	DX,COM	M_PORT_CHA	
594	028B	EC	R3_BUS	SY:	IN	AL,DX	; Input status	
595	028C	24 04		AND	AL,04h			
596	025E	3C 04		CMP	AL,04h		; Check for busy	
597	0260	75 F9		JNZ	R3_BUSY		; Continue if not busy	
598	0262	BA 007C		MOV	DX,DATA_POF	RT_CHA		
599	0265	EC		IN	AL,DX		; Input char from termina	1
600	0266	EE		OUT	DX,AL		; Echo it back to termina	1
601			;					
602	0297	BA 007E	EOI_CO	:MC	MOV DX,C	OM_PORT_	СНА	
603	029A	в0 38		MOV	AL,38h			
604	029C	EE		OUT	DX,AL		; Issue end of interrupt	
605							; command to MPSC	
606			;					
607	029D	B0 A0	EXIT:	MOV	AL,0A0h			
608	029F	BA 0074		MOV	DX,SERIAL_]	[_O_ADRS+	+014h	
609	03A2	EE		OUT	DX,AL		; Issue EOI command to 82	59
610			;					
611	02A3	B0 A0		MOV	AL,0A0h			
612	02A5	BA 00F0		MOV	DX,0F0h			
613	02A8	EE		OUT	DX,AL		; Issue EOI command to sl	ave 8259
614			;					
615	02A9	B0 A0		MOV	AL,0A0h			
616	02AB	BA 00F2		MOV	DX,0F2h			
617	02AE	EE		OUT	DX,AL		; Issue EOI command to ms	tr 8259
618	02AF	CF		IRET				
619	02B0		CSEG	ENDS				
620			;					
621					PAGE			
622	0000		STSEG		SEGMENT	STACK		
623			;					
624	0000	0100 [DB	256 DUP(?)			
625		??						
626]						
627								
628			;					
629	0100		STSEG		SEGMENT	ENDS		
630			;					
631	0000		DSEG		SEGMENT			
632			;					
633	0000	54 45 52 4D	49 4E	STRING	GO DB 'TE	RMINAL ON	NE "Test string'	

634		41	4C	20	4F	4E	45			DB	'11111111111111111'''
635		20	22	54	65	73	74				
636		20	73	74	72	69	6E				
637		67	20	31	31	31	31				
638		31	31	31	31	31	31				
639		31	31	31	31	31	31				
640		31	31	31	22						
641	002E	0 D						DB	0Dh	L	
642	002F	0A						DB	0Ah	L	
643	0030	00						DB	00h	L	
644						;	;				
645	0031	54	45	52	4D	49	4E	STRING	_1	DB	'TERMINAL TWO "Test string'
646		41	4C	20	54	57	4F			DB	'222222222222222222222'''
647		20	22	54	65	73	74				
648		20	73	74	72	69	6E				
649		67	20	32	32	32	32				
650		32	32	32	32	32	32				
651		32	32	32	32	32	32				
652		32	32	32	32	32	22				
653	0061	0 D						DB	0Dh	L	
654	0062	0A						DB	0Ah	L	
655	0063	00						DB	00h	L	
656						;					
657	0064	54	45	52	4D	49	4E	STRING	_2	DB	'TERMINAL THREE "Test string'
657 658	0064	54 41	45 4C	52 20	4D 54	49 48	4E 52	STRING	_2	DB DB	'TERMINAL THREE "Test string' '333333333333333333333"'
657 658 659	0064	54 41 45	45 4C 45	52 20 20	4D 54 22	49 48 54	4E 52 65	STRING	_2	DB DB	'TERMINAL THREE "Test string' '333333333333333333'''
657 658 659 660	0064	54 41 45 73	45 4C 45 74	52 20 20 20	4D 54 22 73	49 48 54 74	4E 52 65 72	STRING	_2	DB DB	'TERMINAL THREE "Test string'
657 658 659 660 661	0064	54 41 45 73 69	45 4C 45 74 6E	52 20 20 20 67	4D 54 22 73 20	49 48 54 74 33	4E 52 65 72 33	STRING	_2	DB DB	'TERMINAL THREE "Test string'
657 658 659 660 661 662	0064	54 41 45 73 69 33	45 4C 45 74 6E 33	 52 20 20 67 33 	4D 54 22 73 20 33	49 48 54 74 33 33	4E 52 65 72 33 33	STRING	_2	DB DB	'TERMINAL THREE "Test string'
657 658 659 660 661 662 663	0064	54 41 45 73 69 33 33	45 4C 45 74 6E 33 33	 52 20 20 67 33 33 	4D 54 22 73 20 33 33	 49 48 54 74 33 33 33 	4E 52 65 72 33 33 33	STRING	_2	DB DB	'TERMINAL THREE "Test string'
657 658 659 660 661 662 663 664	0064	54 41 45 73 69 33 33 33	45 4C 45 74 6E 33 33 33	 52 20 20 67 33 33 33 	4D 54 22 73 20 33 33 33	 49 48 54 74 33 33 33 22 	4E 52 65 72 33 33 33	STRING	_2	DB DB	'TERMINAL THREE "Test string' '33333333333333333"'
657 658 659 660 661 662 663 664 665	0064	54 41 45 73 69 33 33 33 0D	45 4C 45 74 6E 33 33 33	52 20 20 67 33 33 33	4D 54 22 73 20 33 33 33	 49 48 54 74 33 33 33 22 	4E 52 65 72 33 33 33	STRING	_2 0Dh	DB DB	'TERMINAL THREE "Test string' '33333333333333333"'
657 658 659 660 661 662 663 664 665 666	0064 0093 0094	54 41 45 73 69 33 33 33 0D 0A	45 4C 45 74 6E 33 33 33	52 20 20 67 33 33 33	4D 54 22 73 20 33 33 33	49 48 54 74 33 33 33 22	4E 52 65 72 33 33 33	STRING DB DB	_2 0Dh 0Ah	DB DB	'TERMINAL THREE "Test string' '33333333333333333"'
657 658 659 660 661 662 663 664 665 666 667	0064 0093 0094 0095	54 41 45 73 69 33 33 33 0D 0D 0A 00	45 4C 45 74 6E 33 33 33	52 20 20 67 33 33 33	4D 54 22 73 20 33 33 33	 49 48 54 74 33 33 22 	4E 52 65 72 33 33 33	STRING DB DB DB	_2 0Dh 0Ah 00h		'TERMINAL THREE "Test string' '33333333333333333"'
657 658 659 660 661 662 663 664 665 666 667 668	0064 0093 0094 0095	54 41 45 73 69 33 33 33 0D 0A 00	45 4C 45 74 6E 33 33 33	52 20 20 67 33 33 33	4D 54 22 73 20 33 33 33	 49 48 54 74 33 33 22 	4E 52 65 72 33 33 33	STRING DB DB DB	_2 0Dh 0Ah 00h		'TERMINAL THREE "Test string' '33333333333333333"'
657 658 659 660 661 662 663 664 665 666 666 668 669	0064 0093 0094 0095 0096	54 41 45 73 69 33 33 33 0D 0A 00 54	45 4C 45 74 6E 33 33 33 45	52 20 20 67 33 33 33 52	4D 54 22 73 20 33 33 33 4D	49 48 54 33 33 33 22 , 49	4E 52 65 72 33 33 33 33 4E	DB DB DB String	_2 0Dh 0Ah 00h	DB DB LB L L L DB	'TERMINAL THREE "Test string' '33333333333333333333333333333333333
657 658 659 660 661 662 663 664 665 666 667 668 669 670	0064 0093 0094 0095 0096	54 41 45 73 69 33 33 33 0D 0A 00 54 41	45 4C 45 74 6E 33 33 33 45 45	52 20 20 67 33 33 33 52 20	4D 54 22 73 20 33 33 33 33 4D 46	49 48 54 74 33 33 33 22 ; 49 4F	4E 52 65 72 33 33 33 33 4E 55	DB DB DB String	_2 0Dh 0Ah 00h _3	DB DB LB L L L DB DB	'TERMINAL THREE "Test string' '33333333333333333333333333333333333
657 658 659 660 661 662 663 664 665 666 667 668 669 670 671	0064 0093 0094 0095 0096	54 41 45 73 69 33 33 33 0D 0A 00 54 41 52	 45 4C 45 74 6E 33 33 33 45 4C 20 	52 20 20 67 33 33 33 52 20 22	4D 54 22 73 20 33 33 33 33 4D 46 54	 49 48 54 74 33 33 22 49 4F 65 	4E 52 65 72 33 33 33 33 4E 55 73	DB DB DB String	_2 0Dh 0Ah 00h	DB DB LB L L DB DB DB	'TERMINAL THREE "Test string' '33333333333333333333333333333333333
657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672	0064 0093 0094 0095 0096	54 41 45 73 69 33 33 33 0D 0A 00 54 41 52 74	 45 46 74 6E 33 33 33 45 4C 20 20 	52 20 20 67 33 33 33 52 20 22 73	4D 54 22 73 20 33 33 33 33 4D 46 54 74	 49 48 54 74 33 33 22 49 4F 65 72 	4E 52 65 72 33 33 33 33 4E 55 73 69	DB DB String	_2 0Dh 0Ah 00h _3	DB DB DB DB DB	'TERMINAL THREE "Test string' '33333333333333333333333333333333333
657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673	0064 0093 0094 0095 0096	54 41 45 73 69 33 33 0D 0A 00 54 41 52 74 6E	 45 4C 45 74 6E 33 33 33 45 4C 20 20 67 	 52 20 20 20 67 33 33 33 52 20 22 73 20 	4D 54 22 73 20 33 33 33 33 4D 46 54 74 34	 49 48 54 74 33 33 22 49 4F 65 72 34 	4E 52 65 72 33 33 33 33 33 4E 55 73 69 34	DB DB DB String	_2 0Dh 0Ah 00h	DB DB DB DB DB	'TERMINAL THREE "Test string' '33333333333333333333333333333333333
657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674	0064 0093 0094 0095 0096	54 41 45 73 69 33 33 00 00 54 41 52 74 6E 34	 45 46 74 6E 33 33 33 45 4C 20 20 67 34 	52 20 20 67 33 33 33 33 52 20 22 73 20 34	4D 54 22 73 20 33 33 33 33 4D 46 54 74 34 34	 49 48 54 74 33 33 22 49 4F 65 72 34 34 	4E 52 65 72 33 33 33 33 33 4E 55 73 69 34 34	DB DB String	_2 0Dh 0Ah 00h _3	DB DB DB DB DB	'TERMINAL THREE "Test string' '33333333333333333333333333333333333
657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675	0064 0093 0094 0095 0096	54 41 45 73 69 33 33 0D 0A 00 54 41 52 74 6E 34 34	 45 4C 45 74 6E 33 33 33 45 4C 20 20 67 34 34 	 52 20 20 67 33 33 33 52 20 22 73 20 34 34 	4D 54 22 73 20 33 33 33 33 4D 46 54 74 34 34 34	 49 48 54 74 33 33 22 49 4F 65 72 34 34 	4E 52 65 72 33 33 33 33 33 33 33 33 33 33 33 33 33	DB DB DB String	_2 0Dh 0Ah 00h _3	DB DB DB DB DB	'TERMINAL THREE "Test string' '33333333333333333333333333333333333
657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675 676	0064 0093 0094 0095 0096	54 41 45 73 69 33 33 33 0D 0A 00 54 41 52 74 6E 34 34 34	 45 46 74 6E 33 33 33 45 4C 20 20 67 34 34 	52 20 20 67 33 33 33 33 52 20 22 73 20 34 34 34	4D 54 22 73 20 33 33 33 33 33 4D 46 54 54 34 34 34 34	 49 48 54 74 33 33 22 49 4F 65 72 34 34 22 	4E 52 65 72 33 33 33 33 33 33 33 33 33 33 33 33 33	DB DB String	_2 0Dh 0Ah 00h	DB DB DB DB DB	'TERMINAL THREE "Test string' '33333333333333333333333333333333333
657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675 676 677	0064 0093 0094 0095 0096	54 41 45 73 69 33 33 0D 0A 00 54 41 52 74 6E 34 34 34 0D	45 4C 45 74 6E 33 33 33 45 4C 20 67 34 34 34	52 20 20 67 33 33 33 33 52 20 22 73 20 34 34 34	4D 54 22 73 20 33 33 33 33 4D 46 54 74 34 34 34 34	 49 48 54 74 33 33 22 49 4F 65 72 34 34 22 	4E 52 65 72 33 33 33 33 33 33 33 33 33 33 33 33 33	DB DB String DB	_2 0Dh 0Ah 00h _3 0Dh	DB DB DB DB DB DB	'TERMINAL THREE "Test string' '33333333333333333333333333333333333
657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675 675 677 678	00093 0094 0095 0096 0005 0005	54 41 45 73 69 33 33 00 0A 00 54 41 52 74 6E 34 34 0D 0A	45 4C 45 74 6E 33 33 33 45 4C 20 67 34 34 34	52 20 20 67 33 33 33 33 52 20 22 73 20 34 34 34	4D 54 22 73 20 33 33 33 33 33 4D 46 54 54 34 34 34 34	 49 48 54 74 33 33 22 49 4F 65 72 34 34 22 	4E 52 65 72 33 33 33 33 33 33 33 33 33 33 33 33 33	DB DB String DB DB DB	_2 0Dh 0Ah 00h _3 0Dh 0Ah	DB DB DB DB DB DB	'TERMINAL THREE "Test string' '33333333333333333333333333333333333

680	00C8	??	INCHAR	DB	?
681			;		
682	00C9	54 68 69 73 2	0 69 PRNT_S	TRING	DB 'This is a test of the '
683		73 20 61 20 7	4 65		DB 'printer port under intr'
684		73 74 20 6F 6	6 20		
685		74 68 65 20 7	0 72		
686		69 6E 74 65 7	2 20		
687		70 6F 72 74 2	0 75		
688		6E 64 65 72 2	0 69		
689		6E 74 72			
690	00F6	0 D	DB	0Dh	
691	00F7	0A	DB	0Ah	
692	00F8	00	DB	00h	
693	00F9	0000	POINTER_0	DW	0000h
694	00FB	0000	POINTER_1	DW	0000h
695	00FD	0000	POINTER_2	DW	0000h
696	OOFF	0000	POINTER_3	DW	0000h
697	0101	0000	POINTER_4	DW	0000h
698			;		
699	0103	0000 R	BEGIN_0	DW	STRING_0
700	0105	0031 R	BEGIN_1	DW	STRING_1
701	0107	0064 R	BEGIN_2	DW	STRING_2
702	0109	0096 R	BEGIN_3	DW	STRING_3
703			;		
704	010B	0000	TEMP	DW	0000h
705	010D	0000	STORE	DW	0000h
706	010F	00	CHAR	DB	00h
707	0110	00	STO_VEC	DB	00h
708			;		
709	0111	0181 R	INT_VEC_TABLE	2	DW offset RECEIVE_0
710	0113	0193 R		DW	offset RECEIVE_1
711	0115	01A5 R		DW	offset TRANSMIT_0
712	0117	01CD R		DW	offset TRANSMIT_1
713	0119	01ED R		DW	offset PRNT_IN
714	011B	01F8 R		DW	offset PRNT_OUT
715	011D	0227 R		DW	offset TR_8274
716			;		
717	011F	023A R	JMP_TABLE	DW	offset TRANSMIT_CH_B
718	0121	0258 R		DW	offset RECEIVE_CH_B
719	0123	026A R		DW	offset TRANSMIT_CH_A
720	0125	0288 R		DW	offset RECEIVE_CH_A
721	0127		DSEG	ENDS	
722				END	

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SEGMENTS and GROUPS

NAME												SIZE	ALIGN	COMBINE CLAS	S
CSEG .			•						•		•	02B0	PARA	NONE	
DSEG .		•	•		•		•		•	•	•	0127	PARA	NONE	
STSEG									•		•	0100	PARA	STACK	

SYMBOLS

NAME	TYPE	VALUE	ATTR
BEGIN_0	L WORD	0103	DSEG
BEGIN_1	L WORD	0105	DSEG
BEGIN_2	L WORD	0107	DSEG
BEGIN_3	L WORD	0109	DSEG
BUSY	L NEAR	01F8	CSEG
BUSY1	L NEAR	01AC	CSEG
CHAR	L BYTE	010F	DSEG
COM_PORT_CHA	Number	007E	
COM_PORT_CHB	Number	007F	
CR1_0	Number	0027	
DATA_PORT_CHA	Number	007C	
DATA_PORT_CHB	Number	007D	
DELAY1	L NEAR	004E	CSEG
DELAY2	L NEAR	0076	CSEG
EOI_COM	L NEAR	0297	CSEG
EXIT	L NEAR	029D	CSEG
EXIT1	L NEAR	01C8	CSEG
EXIT2	L NEAR	01E8	CSEG
INCHAR	L BYTE	00C8	DSEG
INIT	L NEAR	0000	CSEG
INIT1	L NEAR	000F	CSEG
INT_VEC_TABLE	L WORD	0111	DSEG
JMP_TABLE	L WORD	011F	DSEG
LOOP	L NEAR	016C	CSEG
MR1_0	Number	004E	
MR2_0	Number	0076	
PAR_I_O_ADRS	Number	0078	
POINTER_0	L WORD	00F9	DSEG
POINTER_1	L WORD	00FB	DSEG
POINTER_2	L WORD	00FD	DSEG
POINTER_3	L WORD	OOFF	DSEG

POINTER_4	•	•		•	•	•		L WORD	0101	DSEG
PRNT_IN	•			•	•	•	•	L NEAR	01FD	CSEG
PRNT_OUT	•			•	•	•		L NEAR	01F8	CSEG
PRNT_STRING	•			•	•	•		L BYTE	00C9	DSEG
RO_BUSY	•			•	•			L NEAR	0184	CSEG
R1_BUSY	•			•	•			L NEAR	0196	CSEG
R2_BUSY	•			•	•			L NEAR	025B	CSEG
R3_BUSY	•			•	•			L NEAR	028B	CSEG
RECEIVE_0	•			•	•			L NEAR	0181	CSEG
RECEIVE_1	•			•	•			L NEAR	0193	CSEG
RECEIVE_CH_A .	•			•	•			L NEAR	0288	CSEG
RECEIVE_CH_B .	•			•	•			L NEAR	0258	CSEG
SERIAL_I_O_ADRS	•			•	•			Number	0060	
STORE	•			•	•		•	L WORD	010D	DSEG
STO_VEC	•			•	•	•	•	L BYTE	0110	DSEG
STRING_0	•			•	•	•	•	L BYTE	0000	DSEG
STRING_1	•			•	•	•	•	L BYTE	0031	DSEG
STRING_2	•			•	•	•	•	L BYTE	0064	DSEG
STRING_3	•			•	•			L BYTE	0096	DSEG
STROBEOFF	•			•	•	•	•	Number	000A	
STROBEON	•			•	•	•	•	Number	000B	
TEMP	•			•	•	•	•	L WORD	010B	DSEG
TRANSMIT_0	•			•	•	•	•	L NEAR	01A5	CSEG
TRANSMIT_1	•			•	•	•	•	L NEAR	01CD	CSEG
TRANSMIT_CH_A .	•	•	•	•	•	•		L NEAR	026A	CSEG
TRANSMIT_CH_B .	•	•	•	•	•	•		L NEAR	023A	CSEG
TR_8274	•	•	•	•	•	•		L NEAR	0227	CSEG
VIO_ADRS	•	•	•	•	•	•	•	Number	0070	
VI0_SERVICE								L NEAR	016E	CSEG

Warning Severe

Errors Errors

0 0